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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,695	08/20/2003	Atousa Soroushi	VP075	6704

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EXAMINER	
ELMORE, REBA I	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,695	SOROUSHI, ATOUSA	
	Examiner	Art Unit	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 are presented for examination.

SPECIFICATION

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102

3. The rejection of claims 1-42 as being anticipated by Wollan et al. is ***maintained*** and repeated below with the amended claim language included in the outstanding office action.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1- 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Wollan et al.

6. Wollan teaches the invention (claim 1) as claimed including a method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, the method comprising:

(a) providing at least two registers as using two of the 8-bit registers to form a logical 16-bit register (e.g., see col. 2, lines 16-28);

(b) receiving one byte of a plurality of N-bit bytes that together define an address in the memory space (e.g., see col. 3, line 59 to col. 4, line 61);

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(c) incrementing a count as a result of completing step (b) (e.g., see col. 4, line 62 to col. 5, line 19);

(d) addressing one of the two registers according to the incremented count in step (c) (e.g., see col. 5, lines 11-39); and,

(e) storing the byte in the register addressed in step (d) as there being an input to the register file (e.g., see col. 5, lines 11-39).

As to claim 2, Wollan teaches receiving another byte of the plurality of bytes, resetting the count from step (c), addressing the other of the two registers as a result of the reset count and storing the other byte in the other register as the registers being used as logical registers performing incrementing, decrementing as well as being able to clear (reset) or perform logical operations (e.g., see Table III, col. 13, lines 1-40).

As to claim 3, Wollan teaches (a) receiving a memory access command and (b) accessing the memory space at the address based on the memory access command (e.g., see col. 14, lines 46-65).

As to claim 4, Wollan teaches the memory access command is a write data command (e.g., see col. 14, lines 46-65).

As to claim 5, Wollan teaches the memory access command is a read data command (e.g., see col. 14, lines 46-65).

As to claim 6, Wollan teaches receiving another byte of the plurality of bytes, incrementing the count from step (c) to obtain a next incremented count, addressing the other of the two registers as a result of the next incremented count and storing the other byte in the other

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register inputting data into an A register and then into a B register of the register pair (e.g., see col. 14, lines 46-65).

As to claim 7, Wollan teaches (a) receiving a memory access command and (b) accessing the memory space at the address based on the memory access command (e.g., see col. 14, lines 46-65).

As to claim 8, Wollan teaches the memory access command is a write data command (e.g., see col. 14, lines 46-65).

As to claim 9, Wollan teaches the memory access command is a read data command (e.g., see col. 14, lines 46-65).

As to claim 10, Wollan teaches the 2^M address memory space comprises the address space of a memory device as RAM (e.g., see col. 2, lines 8-16).

As to claim 11, Wollan teaches the 2^M address memory space comprises the address space of a plurality of memory devices as RAM or program memory (e.g., see col. 2, lines 8-46).

7. Wollan teaches the invention (claim 12) as claimed including an apparatus for high speed addressing of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, the apparatus comprising:

(a) at least two registers used as logical registers (e.g., see col. 2, lines 16-28);

(b) a counter as a program counter (e.g., see Figure 9);

(c) a logic circuit adapted for:

(i) receiving one byte of a plurality of N-bit bytes that together define an address in the memory space (e.g., see col. 3, line 59 to col. 4, line 61);

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(ii) incrementing a count of the counter as a result of completing step (i) (e.g., see col. 4, line 62 to col. 5, line 19);

(iii) addressing one of the two registers according to the incremented count in step (ii) (e.g., see col. 5, lines 11-39); and,

(iv) storing the byte in the register addressed in step (iii) as there being an input to the register file (e.g., see col. 5, lines 11-39).

As to claim 13, Wollan teaches the logic circuit is further adapted for receiving another byte of the plurality of bytes, resetting the count of the counter, addressing the other of the two registers as a result of the reset count and storing the other byte in the other register as the registers being used as logical registers performing incrementing, decrementing as well as being able to clear (reset) or perform logical operations (e.g., see Table III, col. 13, lines 1-40).

As to claim 14, Wollan teaches the logic circuit is further adapted for (a) receiving a memory access command and (b) accessing the memory space at the address based on the memory access command (e.g., see col. 14, lines 46-65).

As to claim 15, Wollan teaches the memory access command is a write data command (e.g., see col. 14, lines 46-65).

As to claim 16, Wollan teaches the memory access command is a read data command (e.g., see col. 14, lines 46-65).

As to claim 17, Wollan teaches the logic circuit is further adapted for receiving another byte of the plurality of bytes, incrementing the count of the counter to obtain a next incremented count, addressing the other of the two registers as a result of the next incremented count and

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storing the other byte in the other register inputting data into an A register and then into a B register of the register pair (e.g., see col. 14, lines 46-65).

As to claim 18, Wollan teaches the logic circuit is further adapted for (a) receiving a memory access command and (b) accessing the memory space at the address based on the memory access command (e.g., see col. 14, lines 46-65).

As to claim 19, Wollan teaches the memory access command is a write data command (e.g., see col. 14, lines 46-65).

As to claim 20, Wollan teaches the memory access command is a read data command (e.g., see col. 14, lines 46-65).

As to claim 21, Wollan teaches the 2^M address memory space comprises the address space of a memory device as RAM (e.g., see col. 2, lines 8-16).

As to claim 22, Wollan teaches the 2^M address memory space comprises the address space of a plurality of memory devices as RAM or program memory (e.g., see col. 2, lines 8-16).

8. Wollan teaches the invention (claim 23) as claimed including a machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, the machine having at least two registers where M is greater than N, the method comprising the steps of:

(a) receiving one byte of a plurality of N-bit bytes that together define an address in the memory space (e.g., see col. 3, line 59 to col. 4, line 61);

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(b) incrementing a count as a result of completing step (a) (e.g., see col. 4, line 62 to col. 5, line 19);

(c) addressing one of the two registers according to the incremented count in step (b) (e.g., see col. 5, lines 11-39); and,

(d) storing the byte in the register addressed in step (c) as there being an input to the register file (e.g., see col. 5, lines 11-39).

As to claim 24, Wollan teaches the machine readable medium is adapted for receiving another byte of the plurality of bytes, resetting the count in step (c), addressing the other of the two registers as a result of the reset count and storing the other byte in the other register as the registers being used as logical registers performing incrementing, decrementing as well as being able to clear (reset) or perform logical operations (e.g., see Table III and col. 13, lines 1-40).

As to claim 25, Wollan teaches the machine readable medium is adapted for (a) receiving a memory access command and (b) accessing the memory space at the address based on the memory access command (e.g., see col. 14, lines 46-65).

As to claim 26, Wollan teaches the memory access command is a write data command (e.g., see col. 14, lines 46-65).

As to claim 27, Wollan teaches the memory access command is a read data command (e.g., see col. 14, lines 46-65).

As to claim 28, Wollan teaches the machine readable medium is further adapted for receiving another byte of the plurality of bytes, incrementing the count of the counter to obtain a next incremented count, addressing the other of the two registers as a result of the next

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incremented count and storing the other byte in the other register inputting into an A register and then into a B register of the register pair (e.g., see col. 14, lines 46-65).

As to claim 29, Wollan teaches the method further comprises the steps of (a) receiving a memory access command and (b) accessing the memory space at the address based on the memory access command (e.g., see col. 14, lines 46-65).

As to claim 30, Wollan teaches the memory access command is a write data command (e.g., see col. 14, lines 46-65).

As to claim 31, Wollan teaches the memory access command is a read data command (e.g., see col. 14, lines 46-65).

As to claim 32 Wollan teaches the 2^M address memory space comprises the address space of a memory device as RAM (e.g., see col. 2, lines 8-16).

As to claim 33, Wollan teaches the 2^M address memory space comprises the address space of a plurality of memory devices as RAM or program memory (e.g., see col. 2, lines 8-16).

9. Wollan teaches the invention (claim 34) as claimed including a method for high speed access of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising the steps of:

(a) providing at least two registers, wherein each of the registers contains one of a plurality of N-bit bytes that together define an address in the memory space as using two of the 8-bit registers to form a logical 16-bit register (e.g., see col. 2, lines 16-28);

(b) receiving a memory access command (e.g., see col. 14, lines 46-65) ***that does not specify the registers*** as using other registers in the register file than those cited in the previous step; and,

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(c) accessing the memory space at the address as a result of the memory access command (e.g., see col. 14, lines 46-65).

As to claim 35, Wollan teaches the memory access command is a write data command (e.g., see col. 14, lines 46-65).

As to claim 36, Wollan teaches the memory access command is a read data command (e.g., see col. 14, lines 46-65).

10. Wollan teaches the invention (claim 37) as claimed including an apparatus for high speed access of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, the apparatus comprising:

(a) at least two registers, wherein each of the registers contains one of a plurality of N-bit bytes that together define an address in the memory space as using two of the 8-bit registers to form a logical 16-bit register (e.g., see col. 2, lines 16-28); and,

(b) a logic circuit adapted to receiving a memory access command ***that does not specify the registers*** as using other registers in the register file than those cited in the previous step and accessing the memory space at the address as a result of the memory access command (e.g., see col. 14, lines 46-65).

As to claim 38, Wollan teaches the logic circuit is further adapted so that the memory access is a write data access (e.g., see col. 14, lines 46-65).

As to claim 39, Wollan teaches the logic circuit is further adapted so that the memory access is a read data access (e.g., see col. 14, lines 46-65).

11. Wollan teaches the invention (claim 40) as claimed including a machine readable medium embodying a program of instructions for execution by a machine to perform a method

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for high speed access of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising the steps of:

(a) providing at least two registers, wherein each of the registers contains one of a plurality of N-bit bytes that together define an address in the memory space as using two of the 8-bit registers to form a logical 16-bit register (e.g., see col. 2, lines 16-28);

(b) receiving a memory access command (e.g., see col. 14, lines 46-65) ***that does not specify the registers*** as using other registers in the register file than those cited in the previous step ; and,

(c) accessing the memory space at the address as a result of the memory access command (e.g., see col. 14, lines 46-65).

As to claim 41, Wollan teaches the method is adapted so that the memory access command is a write data command (e.g., see col. 14, lines 46-65).

As to claim 42, Wollan teaches the method is adapted so that the memory access command is a read data command (e.g., see col. 14, lines 46-65).

RESPONSE TO APPLICANT'S REMARKS

12. Applicant's arguments filed March 22, 2006 have been fully considered but they are not persuasive.

13. As to the reference not disclosing or teaching *addressing of a memory space having 2^M addresses using an N-bit bus, where M is greater than N,* this limitation is taught to the extent required by the actual claim language. Wollan specifically teaches using an 8-bit register file for addressing RAM as well as using indirect addressing to access 16-bit address space (e.g., see the summary of the invention).

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14. As to the reference not disclosing or teaching *steps (d) addressing one of the two registers according to the incremented count in step (c) and a step (c) addressing one of the at least two registers according to the incremented count in step (b* , this limitation is taught to the extent required by the actual claim language. Wollan teaches using register-pairs as indirect register pointers for addressing either RAM or program-space using 16-bit addresses by either incrementing or decrementing to use adjacent registers thereby providing a high-byte and a low-byte for the memory access for 16-bit operations (e.g., see col. 5, lines 6-38).

15. As to the reference not disclosing or teaching *a logic circuit adapted for: (iii) addressing one of the two registers according to the incremented count in step (ii)* or more specifically *that registers are addressed according to the incremented count*, this limitation is specifically taught as stated above.

16. As to the reference not disclosing or teaching *a memory access command that does not specify the claimed at least two registers*, this limitation is taught to the extent required by the actual claim language. This limitation merely states the system has the capability of receiving a memory access command utilizing registers other than the two registers previously claimed. As the register file has a plurality of registers, not just two registers, this limitation is specifically taught.

Office Action Finality

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

CONCLUSION

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday or Wednesday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2189

Thursday, June 08, 2006

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